Visit **www.brpaper.com** for downloading previous years question papers of B-tech,Diploma,BBA,BCA, MBA,MCA,Bsc-IT,M-Tech,PGDCA,B-com

	1						
	1						
Roll No							
$\mathbf{N}\mathbf{U}\mathbf{H} \perp \mathbf{V}\mathbf{U}$							

Total No. of Questions: 09

Total No. of Pages: 02

B.Tech.(ECE/ETE)(Sem.6) VLSI DESIGN Subject Code: BTEC-604 Paper ID: A2318

Time: 3 Hrs.

Max. Marks: 60

K.CC

INSTRUCTION TO CANDIDATES:

- 1. Section A is COMPULSORY consisting of TEN Questions carrying TWO marks each.
- 2. Section B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
- **3.** Section C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION A

- 1. Write in brief
 - a) Explain the types of delays in VHDL
 - b) Compare between function and procedure
 - c) What are PULL UP and PULL DOWN networks
 - d) How is generic statement useful in VHDL code
 - e) Differentiate between signal and variable
 - f) Write and explain VHDL code using CASE statement
 - g) Differentiate between library and package
 - h) Describe if else statement
 - i) Write the VHDL code for half adder
 - j) What is power dissipation

SECTION B

- 2. Explain shift and rotate operations in VHDL with example
- **3.** Explain the switching characteristics delay model
- 4. Write the VHDL code for 3 bit Binary to Gray converter.

| M71124

- 5. Write the VHDL code for 8: 3 decoder using if else statement
- 6. What is scaling. What is the effect of scaling on the circuit performance

SECTION C

- 7. Write VHDL code for 3- bit binary asynchronous up converter
- **8.** Draw CMOS inverter. Discuss its DC characteristics. Write the condition for the different region of operations
- 9. Write the VHDL code for 8:1 MUX using structural modeling

	com	
20	er.	com
6re	apel	
	V V	