Roll No.

Total No. of Questions: 09 **Total No. of Pages: 02**

B. Tech. (3D ANIMATION) (Sem. 3)
COMPUTER ARCHITECTURE
Subject Code: BTCS-301
Paper ID: A1123

Time: 3 Hrs. **Max. Marks: 60**

INSTRUCTIONS TO CANDIDATES:

1. **Section A is COMPULSORY consisting of TEN Questions carrying TWO marks each**
2. **Section B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **Section C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION A

1. Answer briefly:

a) What is a Flip Flop?
b) What is a Multiplexer?
c) What is a virtual memory?
d) What is the role of a register?
e) How many types of registered are there?
f) What is an Instruction Cycle?
g) What is an auxiliary memory?
h) What is the difference between serial and parallel processing?
i) What is the use of DMA?
j) What is the need of a stack in processing?

SECTION B

2. Design a combinational circuit that generates 9's complement of a BCD digit.

3. Show that the dual of EX-OR is also its complement.

4. Explain with the help of an example, the use of hamming code as error detection and correction code.

5. With the help of a neat sketch, explain the working of a 4-bit universal shift register.

6. State the condition in which overflow occurs in case of addition & subtraction of two signed 2's complement number. How is it detected?

SECTION C

7. Give the hardware organization of associative memory. Why associative memory is faster than other memories. Deduce the logic equation used to find the match in the associative memory. Explain how four-bit argument register is realised.

8. a) Give the flow chart for add and .subtract operation of two signed 2's complement data. Explain the logic of each operation.

b) Give the flow chart for add and subtract operation of two signed 2's complement data. Explain the logic of each operation

9. a) Why page-table is required in a virtual memory system. Explain different ways of organizing a page table.

b) Design a sequential circuit with JK flip-flop to satisfy the following state equations. A(t+l) = A'B'CD + A'B'C + ACD +AC'D' B(t+l) = A'C +CD'++ A'BC' C(t+l) = B D (t+1) = D'

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