Roll No. | | | | | | | | | | | |

Total No. of Questions: 09 **Total No. of Pages: 02**

B. Tech. (CSE) (Sem. 3)
COMPUTER ARCHITECTURE
Subject Code: CS-201
Paper ID: A0451

Time: 3 Hrs. **Max. Marks: 60**

INSTRUCTIONS TO CANDIDATES:

1. **Section A is COMPULSORY consisting of TEN Questions carrying TWO marks each**
2. **Section B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **Section C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION A

1.

a) What is the difference between hardware interrupt and software interrupt?

b) What are superscalar processors?

c) By which method 8085 microprocessor carryout the subtraction.

d) Which method is used for resolving resource conflict by the compiler itself?

e) How many read and write cycles are generated by 8085 to execute the OUT port instruction?

f) Give examples for SIMD and MIMD based architectures?

g) How Look Ahead carry generator speeds up the processing?

h) How is the evaluation of Computer Architecture done?

i) Define Virtual Memory.

j) The time delays for the four segments in a pipeline are as follows: t_1 = 50ns, t_2 = 30ns, t_3 = 95ns, and t_4 = 45ns. The interface registers delay time t_r = 5ns. How long would it take to add 100 pairs of numbers in the pipeline?

SECTION B

2. Compare the instruction set Architecture of RISC and CISC processor for the instruction formats, addressing modes and cycle per instruction (CPI).

3. What are Transaction Processing Benchmarks? What for are they used?

4. Discuss in brief the various I/O modes?

5. What are reasons of pipeline conflicts in pipelined processor? How are they resolved?

6. How is interaction with operation system done using Serial-Parallel interfaces.

SECTION C

7. The computer uses a memory unit with 256K words of 32 bit each. A binary instruction code is stored in one word of memory. The instruction has four parts; indirect bit, an operation code, a register code part to specify one of the 64 registers, and an address part.

a) How many bits are there in an operation code, the register code and address part?
b) Draw the instruction word format and indicate the number of bits in each part.
c) How many bits are there in the data and address inputs of the memory?

8. Give the significance of layered architecture. Write short note on cost/ benefits in a layered architecture design.

9. Give the hardware organization of associative memory. Why associative memory is faster than other memories. Deduce the logic equation used to find the match in the associative memory. Explain how four-bit argument register is realized.