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B.Tech. (Sem. - 3rd)

COMPUTER ARCHITECTURE

SUBJECT CODE : CS - 201

Paper ID : [A0451]

[Note : Please fill subject code and paper ID on OMR]

Time : 03 Hours **Maximum Marks : 60**

Instruction to Candidates:

1) Section - A is **Compulsory**.
2) Attempt any **Four** questions from Section - B.
3) Attempt any **Two** questions from Section - C.

Section - A

Q1) *(10 x 2 = 20)*

a) Convert the following logic function into minterm

$$ABC'DE' + AB'C'DE' + ABCDE' + AB'CD'E'$$

b) Define the terms real time computer & process control computer.

c) Give the layered view of a computer system.

d) What is the role of Shift Registers in digital computers?

e) Perform the subtraction with the following unsigned binary number by taking the 2's compliment of the subtrahend

1010100 - 1010100

f) Explain the meaning of the memory - reference instruction STA.

g) What is the difference between micro program and micro code?

h) What do you mean by software interrupt?

i) How Cache Memory is useful in memory hierarchy?

j) What do you mean by Interrupt - initiated I/O concept?

Section - B

(4 x 5 = 20)

Q2) Explain in brief about MIMD machines.

Q3) Give an overview of CISC Architecture.

Q4) A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory - mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers. Give the address range in hexadecimal for RAM, ROM, and interface.

Q5) A DMA controller transfers 16 - bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU be slowed down because of the DMA transfer?

Q6) Discuss the hardware implementation of division for signed-magnitude data.

Section - C

(2 x 10 = 20)

Q7) Explain in detail the main features of at least two performance evaluation benchmarks.

Q8) (a) Explain why poor load balancing leads to less-than-linear speedup?

(b) A given processor has 32 registers, uses 16-bit immediates, and has 142 instructions in its ISA. In a given program, 20% of the instructions take one input register and have one output register, 30% have two input registers and one output register, 25% have one output and one input register and take an immediate input as well, and the remaining 25% have one immediate input register and one output register. For each of the four types of instructions, how many bits are required? Assume that the ISA requires that all instructions be a multiple of 8 bits in length.

Q9) (a) How does pipelining improve performance?

(b) What is the result of the following operations when executed on a 8-bit processor that uses a 2's complement representation for negative integers?

LSH 14, 3

ASH 17, 5

LSH –23, –2

ASH –23, –2