May 2005

Section - A (Marks : 2 each)

- Convert the following logic function into minterm A'BC'D'E'F + A'BC'DEF' + AB'C'DEF' + AB'C'DEF' - ABC'DE'F'
 - Define the terms I/O processor and I/O controller.
 - Give the layered view of a computer system.
 - What is the role of Binary Counters in digital computers?
 - Perform the subtraction with the following unsigned binary number by taking the 2's complement of the subtrahend 11010-11111.
 - Explain the meaning of the memory-reference instruction BUN.
 - What is the difference between micro code and micro instruction?
 - Give two examples of program control instructions.
 - How Virtual Memory is useful in memory hierarchy?
 - What do you mean by programmed I/O Concept?

Section - B (Marks: 5 each)

- Q. 2 What is the significance of LINPACK benchmark specifications?
- **Q**. 3 Give an overview of 8255 programmable ports.
- Q. 4 A computer uses RAM chips of 1024 x 1 capacity. How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes? Also explain in words how the chips are to be connected to the address bus?
- Q. 5 How many characters per second can be transmitted over a 1200-band line in each of the following modes considering a character code of 8 bits:
 - Synchronous serial transmission.
 - Asynchronous serial transmission with 2 stop bit.
- Discuss Booth Multiplication algorithm with the help of suitable Q. 6 example.

detail how Direct Memory Access system works by **Milable example showing the various stages.**

two examples of problems that could occur it a computer wild user programs to access I/O devices directly, rather than requiring them to go through the operating system.

Use II.EE single-precision floating point numbers to compute the following quantities:

1125 +45

0 125 * 8

- Explain why poor load balancing leads to less than linear speedup.
 - How many bits of storage are required for the tag array of 32-KB cache with 256-byte eache lines and four-way-set-associativity if the cache is write-back but does not require any additional bits of data in the tag array to implement the write-back policy? Assume that the system containing the cache uses 32-bit addresses.