May 2007

## Section - A (Marks : 2 each)

Q 1 (a) Define Addressing Modes. What are the different types of addressing modes ?

(b) Difference between Computer Architecture and computer organization.

(c) What do you mean by instruction parallism ?

(d) Write any four "Zero Byte" instruction.

(e) Differentiate between RISC and CISC processors.

(f) Differentiate between block and pages.

(g) Write two techniques to implement Virtual Memory ?

(h) What is the difference between physical address and logical address ?

(i) Why floating point representation is preferred over fixed point representation.

(j) What is the basic difference between a branch instruction, a call subroutine instruction and program interrupt.

## Section - B (Marks : 5 each)

Q 2 What are system attributes to prefromance ? How do we calculate MIPS rate and throughput rate ?

Q 3 Explain addition subtraction algorithm with signed magnitude data, also give the hardware implementation.

Q 4 A computer has 32-bit instruction and 12-bit address. If there are 250 two address instructions, how many one address instructions can be formulated.

Q 5 Convert the following numerical arithmetic expression into reverse polish notation and show the stack operation for evaluating the numerical results.

(3 + 4) [10 (2 + 6) + 8]

Q 6 Explain the difference between Hardwired control and micro programmed control. Is it possible to have hardwired control associated with a control memory.

## Section - C (Marks : 10 each)

Draw the schematic diagram of interfacing 8251 A with 8085. Interconnections should be such as to get port address for control register and data register as 89H and 88H respectively.

Q 8 (a) A DMA controller transfers 16-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU will be slowed down because of the DMA transfer.

(b) Define benchmarks ? Name and explain the benchmarks available for performance evaluation.

Q 9 Describe the following terminology associated with multiprocessor :

(a) Mutual Exclusion

(b) Critical Section

(c) Hardware Lock

(d) Semaphores

(e) Test and Set instruction

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