Roll No. .................        Total No. of Pages : 02

Total No. of Questions : 09

# B.Tech.(CSE/IT) (Sem.–3)
## COMPUTER ARCHITECTURE
### Subject Code : CS-201
### Paper ID : [A0451]

Time : 3 Hrs.        Max. Marks : 60

**INSTRUCTION TO CANDIDATES :**
1. SECTION-A is COMPULSORY.
2. Attempt any FOUR questions from SECTION-B.
3. Attempt any TWO questions from SECTION-C.

**SECTION-A**        **(8 × 2.5 = 20 Marks)**

1.  (a) What are the advantages of interrupts in computers ?

    (b) What is the need for a cache memory ? Where is it located in a computer ?

    (c) A given program consists of 50 instruction loop that is executed 35 times. It takes 6,000 cycles to execute the program on a given system. Find the computer performance in CPI (cycles per instruction).

    (d) What do you understand by programmed I/O ?

    (e) What do you understand by I/O channel ?

    (f) What is Superscalar machine ?

    (g) List the functions of 8251.

    (h) What do you understand by the terms "loosely coupled" and "tightly coupled" in parallel computers ?

**[A-12]1324/1330**

**SECTION-B**          **(4 × 5 = 20 Marks)**

2. With the help of a flow chart discuss the process of subtraction of floating point numbers. Also explain the issues involved in its hardware implementation.

3. What is the need of control unit in computer ? Draw the control unit of a basic computer. Discuss how fetch and decode phases are carried out.

4. Describe the principle of operation and role of Stack memory in program execution. State the microinstructions executed in stack operation.

5. Describe in detail the Daisy- chaining priority to handle interrupts with suitable example.

6. Discuss the functions of DMA controller in data transfer between I/O & memory.  Also state different modes of DMA operation.

**SECTION-C**          **(2 × 10 = 20 Marks)**

7. Use Booth multiplication algorithm to multiply 25 with 8. Show all the steps clearly.

8. A task can be carried out with a six stage pipeline with clock cycle of 8 ns.  The same task can be done in a non pipeline unit in 40 *ns*. Determine the speed up ratio of the pipeline for 120 tasks. What is the maximum speed up that can be achieved ? Determine the number of clock cycles it takes to process 220 tasks.

9. Write short notes on the following :

(a) Transaction processing bench marks

(b) SPMD