Roll No..... Total No.of Pages:01

BTECH, SEM 3RD –2014

COMPUTER ARCHITECTURE

Paper Code (CS-201)

Paper Id. [A0451]

MM: 60 TIME: 3 HRS.

Note: Attempt the questions from sections A and B as per the instructions given in the respective sections.

SECTION – A (Compulsory) Attempt all parts.

1 (a) What do you understand by fixed point arithmetic? (8*2.5=20)
(b) Differentiate between hardwired and software interrupt.
(c) What are the functions of fast adders?
(d) How many clock cycles are required to process 200 tasks in eight segment pipeline?
(e) What is CISC?
(f) List some properties of MIMD.
(g) Differentiate between single-processor machine and multiprocessor machines.
(h) What are the issues in CPU design?

SECTION – B (Attempt any four questions.)

2. How addition and subtraction is performed with signed 2's complement data? Explain the hardware implementation and algorithm for it. 05

3. Why can you not connect I/O devices directly to a system bus? Explain. 05

4. Show how data transfer from disk to memory is conducted under programmed I/O, interrupt-driven I/O, and DMA I/O schemes. 05

5. Explain and show diagrammatically how address sequencing is done in hardwired programmed control unit. 05

6. What do you understand by I/O channels? Discuss the importance of it. 05

SECTION – C (Attempt any two questions.)

7. What are the benchmarks for evaluating the performance of a multiprocessor system (SIMD)? Explain with example. 10

8. What do you understand by cache coherence problem? What are the solutions to the cache coherence problem? Explain. 10

9. Write short notes on the following: 10
(a) I/O performance measure
(b) 8251 chip

----------END----------