## Paper ID [A0453]

(Please fill this Paper ID in OMR Sheet)

## B. Tech. (Sem. $-3^{\text {rd }}$ )

DIGITAL CIRCUITS \& LOGIC DESIGN (CS - 205)
Time : 03 Hours
Maximum Marks : 60
Instruction to Candidates:

1) Section - A is Compulsory.
2) Attempt any Four questions from Section - B.
3) Attempt any Two questions from Section - C.

## Section - A

Q1)

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(10 \times 2=20)
$$

a) The decimal equivalent of Binary number 11010 is
(A) 26
(B) 36
(C) 16
(D) 23
b) 1's complement representation of decimal number of -17 by using 5 bit representation is
(A) 11101110
(B) 11011101,
(C) 11001100
(D) 00010001
c) The excess 3 code of decimal number 26 is
(A) 01001001
(B) 01011001
(C) 10001001
(D) 01001101
d) How many AND gates are required to realize $\mathrm{Y}=\mathrm{CD}+\mathrm{EF}+\mathrm{G}$
(A) 4
(B) 5
(C) 3
(D) 2
e) How many select lines will a 16 to 1 multiplexer will have
(A) 4
(B) 3
(C) 5
(D) 1 .
i) How many flip flops are required to construct a decade counter
(A) 10
(B) 3
(C) 4
(D) 2
g) Which TTL logic gate is used for wired ANDing
(A) Open collector output
(B) Totem Pole
(C) Tri state output
(D) ECL gates
h) CMOS circuits consume power
(A) Equal to TTL
(B) Less than TTL
(C) Twice of TTL
(D) Thrice of TTL
i) IC 7490 contains flip flops
(A) 4
(B) 3
(C) 2
(D) 10
j) • In a RAM, information can be stored
(A) By the user, number of times.
(B) By the user, only once.
(C) By the manufacturer, a number of times.
(D) By the manufacturer only once.

## Section - B

$(4 \times 5=20)$
Q2) (a) Convert decimal 177.25 to octal number.
(b) Perform following subtraction
(i) 11001-10110 using l's complement.
(ii) 11011-11001 using 2's complement.

Q3) (a) Reduce the following equation using k-map $Y=\overline{A B} \bar{C}+A \bar{C} \bar{D}+A \bar{B}+A B C \bar{D}+\overline{A B} C$.
(b) Write the expression for Boolean function
$F(A, B, C)=\Sigma \mathrm{m}(1,4,5,6,7)$ in standard POS form.

Q4) Explain working of three state TTL.
Q5) What do you mean by interfacing? Explain its need. How will you interface TTL to CMOS?

Q6) (a) Implement the following function using a 3 line to 5 line decoder
$\mathrm{S}(\mathrm{A}, \mathrm{B}, \mathrm{C})=\Sigma \mathrm{m}(1,2,4,7)$
$C(A, B, C)=\Sigma m(3,5,6,7)$.
(b) How will you form an 5 bit adder using 2 four bit adder IC's 7453 .

## Section-C

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(2 \times 10=20)
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Q7) (a) Explain the operation of octal to binary encoder.
(b) Explain the working of master slave JK flip flop.

Q8) (a) Explain how parallel In Serial Out (PISO) shift register works.
(b) Design a mod-6 up counter.

Q9) (a) Explain how EPROM memory cell works.
(b) Explain the working of dual slope $A / D$ converter.

