Roll No. _____

[No. of Questions : 09] [Total No. of Pages : 02

B.Tech. (Sem. - 3rd)

DIGITAL CIRCUITS AND LOGIC DESIGN

SUBJECT CODE : CS - 205

Paper ID : [A0453]

[Note : Please fill subject code and paper ID on OMR]

Time : 03 Hours Maximum Marks : 60

Instruction to Candidates:

1) Section - A is **Compulsory**.
2) Attempt any **Four** questions from Section - B.
3) Attempt any **Two** questions from Section - C.

Section - A

(10 × 2 = 20)

a) How many select lines are required for a 10 to 1 MUX?

b) List the various types of A/D converters.

c) How ROM is different from RAM?

d) Divide $(10101011)_2$ by $(101)_2$.

e) Construct the truth table for $Z = xy + \overline{xy}$

f) If A =1010 and B = 1001, find A - B using 2's complement method.

g) How sequential circuits are different from combinational circuits?

h) Compare TTL with ECL.

i) Compare synchronous counters with asynchronous counters.

j) Minimize the following expressions

(i) $A + \overline{(\overline{B} + \overline{C})}$

(ii) $\overline{(A\overline{B}(C + \overline{D}) + \overline{C})}$

Section - B

(4 × 5 = 20)

Q2) Minimize the following expressions using K - map

(a) $Y = (A + B)(A + \overline{B})(A + \overline{C})$

(b) $Y = \overline{A}B + A\overline{B}C + AB$

Q3) Design 8:1 MUX by using two 4:1 MUX.

Q4) What is race around condition? How it is avoided in Master Slave Flip Flop?

Q5) Explain the working of successive approximation A/D converter.

Q6) Write a short note on the following:

(a) CMOS

(b) RTL

Section - C

(2 × 10 = 20)

Q7) (a) Design full adder using logic gates.

(b) Design EX - OR gate using NAND gates only.

Q8) Design mod - 8 synchronous counter using T flip flops.

Q9) Explain the different types of ROMs. Discuss their advantages and disadvantages