Roll No. ....

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B.Tech. (Sem. - 3rd)
DIGITAL CIRCUITS AND LOGIC DESIGN
SUBJECT CODE : CS - 205
Paper ID : [A0453]

[Note : Please fill subject code and paper ID on OMR]

Time : 03 Hours   Maximum Marks : 60

Instruction to Candidates:

1)   Section - A is **Compulsory.**

2)   Attempt any **Four** questions from Section - B.

3)   Attempt any **Two** questions from Section - C.

Section - A

Q1)   (10 × 2 = 20)

a)   Convert binary number 1001 into gray.

b)   Find SOP form of $f = AB + BC + \overline{A}$.

c)   Implement half subtractor using NAND gates.

d)   Find % age resolution of a 12 bit BCD input D/A converter which has full scale o/p of 29.97 V.

e)   Convert a D flip flop into a T flip flop.

f)   Differentiate between Asynchronous counter and Synchronous counter.

g)   What is significance of figure of merit of flip flops.

h)   Design a 4 : 1 mux.

i)   Classify logic families on the basis of number of gates on a single chip.

j)   Write pros and cons of SRAM and DRAM cell.

Section - B

(4 × 5 = 20)

Q2) Design a combinational ckt with 3 inputs and 1 output. The output is high only when more than one input is high.

Q3) Design a MOD 6 counter using T-flip flops.

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Q4) What are multivibrator circuits. Explain Astable multivibrator with the help of circuit diagram.

Q5) Explain the operation of two input TTL NAND gate.

Q6) Using Boolean Algebra show that

$$(A+B)(\overline{A}+C)(B+C) = AC + B\overline{A}$$

Section - C

(2 × 10 = 20)

Q7) Design a comparator circuit which compares two 2 bit numbers. It has three outputs A > B, A < B and A = B. Also show that $A < B = \overline{A > B} \cdot \overline{A = B}$.

Q8) Design a three bit, MOD 6, unit distance up-down counter.

Q9) What are programmable logic devices. What are their advantages. Explain in detail the architecture of a programmable logic device.

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