Roll No. | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech.(CSE/IT) (Sem.–3rd)

DIGITAL CIRCUITS AND LOGIC DESIGN

Subject Code : BTCS-303 (2011 Batch)

Paper ID : [A1125]

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students has to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students has to attempt any TWO questions.**

SECTION-A

1. Write briefly :

a) State DeMorgan's theorems.

b) What is a Multiplexer Tree?

c) Differentiate Combinational and Sequential Circuits.

d) What do you mean by weighted code? Give example.

e) What is universal shift register?

f) How many flip flops are required for Mod-6 Counter?

g) Differentiate Static RAM and Dynamic RAM.

h) What is the importance of parity bit ?

i) Determine the resolution of the output from a DAC that has a 12-bit input.

j) Differentiate Moore and Mealy Machines.

SECTION-B

2. What is a Decoder? Compare a decoder and a demultiplexer with suitable block diagrams.
3. Draw the circuit of a counter type A-D converter and explain its operation.
4. Design a full adder circuit using NAND gates only.
5. Draw the circuit diagram of a mod-5 synchronous counter.
6. Simplify the following expression using K-Map :

   $f(A,B,C,D) = \Sigma m(0, 3, 4, 5, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$.

SECTION-C

7. What is Race around Condition? How it can be avoided? Also Discuss the working of Master Slave J-K Flip Flop.
8. Discuss the comparison of the important features of various IC logic families. Also draw and explain the operation of TTL NAND Gate.
9. Write a note on following :
   a) Canonical POS
   b) Boolean algebra.
   c) Magnitude Comparator
   d) Excess-3 Code.