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MAY-2014

B. Tech. CSE(Sem. – 3rd)

DIGITAL CIRCUITS & LOGIC DESIGN (BTCS - 303)

Time: 03 Hours **Maximum Marks : 60**

Instruction to Candidates:

1) Section - A is **Compulsory**.

2) Attempt any **Four** questions from Section - B.

3) Attempt any **Two** questions from Section - C.

Section – A

Q1) **(10x2=20)**

a). Find the signed 8-bit binary number equivalent to 7_{10}.

b). How many AND gates are required to realize Y = ACD + EF + GH

c). What is the difference between synchronous and asynchronous?

d). What do you understand by nonvolatile memory?

e). What is the use of EEPROM?

f). Write the name of various types of Digital to Analog Convertors.

g). What is the difference between edge triggering and level triggering?

h). What is the use of static RAM?

i). Define racing problem in JK-Flip flop.

j). Write one advantage of CMOS logic family.

Section – B

(4x5=20)

Q2) State and prove De-Morgan's theorems.

Q3) Draw and explain the operation of TTL inverter.

Q4) Implement the function $f(w, x, y, z) = m(0, 1, 5, 7, 8, 10, 13, 14, 15)$ using two 8-way multiplexers with an active low enable, plus an OR gate.

Q5) Explain the working of ladder type Digital to Analog Convertor.

Q6) Write a short note on Field Programmable Gate Array.

Section – C

(2x10=20)

Q7) Find the minimum sum of products expression for the function

f(a, b, c, d) = $\Sigma m(1, 3, 4, 6, 7, 9, 11, 12, 13, 15)$ using QM method.

Q8) Design a MOD - 10 synchronous counter using J-K Flip-Flops. Explain its working with the help of timing diagram.

Q9) Discuss various types of Read only Memories in detail.

————End————