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Total No. of Questions : 09] **[Total No. of Pages : 01**

B.Tech. (Sem. 3rd)

DIGITAL CIRCUITS & LOGIC DESIGN

SUBJECT CODE : CS - 205

Paper ID : [A0453]

[Note : Please fill subject code and paper ID on OMR]

Time : 03 Hours **Maximum Marks : 60**

Instruction to Candidates:

1) Section - A is **Compulsory**.
2) Attempt any **Four** questions from Section - B.
3) Attempt any **Two** questions from Section - C.

Section - A

Q1) ***(10 × 2 = 20)***

a) Perform subtraction of 100 with 99 using 1's complement.
b) How many full adders are required to construct an m-bit parallel adder?
c) What is the meaning of universal gates?
d) What is the use of Multiplexer?
e) What are synchronous counters?
f) How many pulses are needed to change the contents of a 8 bit up – counter from 10101100 to 00100111?
g) Realize NOT gate using NAND and NOR Gates separately.
h) Convert 1234 Octal number to hexadecimal number.
i) What is the 2's complement representation of $(-539)_{10}$ in hexadecimal?
j) Describe the advantages of CMOS Memory chips.

Section - B

(4 × 5 = 20)

Q2) State and Prove the De Morgan's Theorem.

Q3) Draw a K-Map for a Function of four variables F(A, B, C, D) such that $F = \sum m(0, 1, 4, 5, 3, 2, 11, 10)$ and use it to reduce this function.

Q4) Explain how division can be accomplished by repeated subtraction.

Q5) Draw a logic diagram and waveform for mod – 5 counter.

Q6) What are PROMs? How data can be erased from PROM?

Section - C

(2 × 10 = 20)

Q7) Explain the Design the Stair-step Ramp A/D Converter. How performance of various A/D converters is measured?

Q8) (a) Design a Diode matrix RAM for conversion of BCD to excess-3 code.
(b) How controlled Buffer Registers are designed?

Q9) (a) Explain why does CMOS or TTL perform better in high noise environment.
(b) Draw and explain the Schottky TTL NAND Gate and its uses.