Total No. of Questions: 09

B.Tech.(CSE/IT) (2011 onwards) / B.Tech.(3D Animation & Graphics) (2012 onwards) (Sem. – 3)

COMPUTER ARCHITECTURE

M Code: 56591

Subject Code: BTCS-301

Paper ID: [A1123]

Time: 3 Hrs. **Max. Marks: 60**

INSTRUCTIONS TO CANDIDATES:

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION A

1. a) What is meant by RTL?

   b) What is three address instruction format?

   c) Compare RISC with CISC architecture.

   d) What is write-through cache?

   e) Discuss shift micro operations.

   f) Name the registers generally contained in the processor.

   g) What are memory reference instructions?

   h) Discuss addressing modes.

   i) What is Inter processor communication?

   j) Write the use of Priority Interrupt.

SECTION B

2. List and explain the steps involved in the execution of a complete instruction?
3. What is the difference between a hardwired control unit and a micro programmed control unit? Explain the relative advantages of each.
4. List the advantage of cache in computer architecture. Discuss write through and write back cache techniques.
5. Explain the operation of DMA using a block diagram. Give an example application of DMA data transfer.
6. Explain direct and indirect register addressing mode with suitable example.

SECTION C

7. What is meant by associative memory? Explain briefly the hardware organization of such a memory.
8. Write short note on following
   a) Vector processors
   b) Instruction format
9. What do you understand by Instruction Pipeline? Mention the stages of Pipeline.