Total No. of Questions: 09

B.Tech. (CSE) / (IT) (Sem. – 3)

COMPUTER ARCHITECTURE

M Code: 56501

Subject Code: CS-201

Paper ID: [A0451]

Time: 3 Hrs. **Max. Marks: 60**

INSTRUCTIONS TO CANDIDATES:

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION A

1. a) Differentiate between computer architecture and computer organization.

   b) Which types of signals are necessary to activate the external interrupts of 8085?

   c) What is the advantage of relative addressing mode?

   d) Why DMA controller has a bidirectional address bus?

   e) Define SPMD.

   f) What are the two instructions needed in the basic computer in order to set E flip flop.

   g) What must the address field of an indexed addressing mode instruction be to make it same as a register indirect mode instruction?

   h) A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500. Determine the relative address value in binary using 12 bits.

   i) Briefly explain an instruction format.

   j) Give an example of delayed branch with the three-segment pipeline.

SECTION B

2. What is the difference between set-associative mapping and fully associative mapping? Can we implement a 3-way set associative cache?
3. What is the difference between programmed I/O, interrupt driven I/O and DMA?
4. Formulate a mapping procedure that provides eight consecutive microinstructions for each routine. The operation code has 6 bits and the control memory has 2048 words
5. Why is it difficult to implement a hardwired control unit for modern CISC processors? Justify.
6. Is cache memory must for any pipelined architecture? Justify.

SECTION C

7. Explain the following paradoxical statement: The throughput of a pipeline processor can sometimes be maximized by judiciously inserting the delays in pipelines in put data stream.
8. A computer uses a memory of 65,536 words with eight bits in each word. It has the following registers: PC, AR, TR (16 bits each), and AC, DR and IR (eight bits each). A memory reference instruction consists of three words: an eight bit operation code (one word), and a 16- bit address in the next two words). All the operands are of eight bits. There is no indirect bit.
   a) Draw a block diagram of a computer showing the memory and registers.
   b) Draw the diagram showing the placement in memory of a typical three-word instruction and corresponding 8-bit operand.
   c) List the sequence of the micro-operations for fetching a memory reference instruction and then placing the operand in DR. Start from the timing signal T_0. [3+3+4=10M]
9. Explain the difference between hardwired control and micro programmed control. Is it possible to have a hardwired control associated with the control memory?