Total No. of Questions: 09

B.Tech. (ECE) / (ETE) (2011 Onwards) (Sem. – 6)

VLSI DESIGN

M Code: 71124
Subject Code: BTEC-604
Paper ID: [A2318]

Time: 3 Hrs. **Max. Marks: 60**

INSTRUCTIONS TO CANDIDATES:

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION A

1. a) What is an entity? Give one example.

   b) What is transport delay? How it differs from inertial delay?

   c) Explain subtype for any data type with an example.

   d) What is the significance of process statement?

   e) What is configuration declaration?

   f) Define constant voltage scaling.

   g) Why NMOS is called as pull-down network?

   h) What is resolution function?

   i) Why NMOS technology is preferred more than PMOS technology?

   j) Perform the following using *sra2* and *sll3* shift operators:

      i) 10101101

      ii) 01011110

SECTION B

2. Differentiate between concurrent and sequential statements in VHDL with examples.
3. Derive the current equation for a p-channel MOS transistor operating in the linear region, i.e., for $V_{SG} + V_{TP} > V_{SD}$.
4. Write a VHDL code in structural style of modeling for SOP for the following expression:

   $F = \sum m (1,4,6,8,9,11,12,14,15) + \sum d(2,5,7)$
5. What are data objects? Explain any two with example.
6. Describe the CZ method for wafer formation in CMOS process.

SECTION C

7. Sketch the cross section and explain the operation of n-channel enhancement type MOS transistor. Draw the characteristics of the device. How many diffusion steps are required to form it?
8. Describe various logic operators used in VHDL language with two examples of each.
9. Write a VHDL code for 4-bit Binary to Gray code converter using behavioral style of modeling.