Roll No _____ Total no of page-2

Examination May-2014

B.Tech-ECE
VLSI DESIGN
Subject Code: BTEC-604

Time: 03 Hours **Maximum Marks: 60**

Instruction to Candidates:
Section-A is compulsory consisting of ten questions carrying two marks each.
Section-B consists of five questions carrying five marks each and students have to attempt any four questions.
Section-C contains three questions carrying ten marks each and students have to attempt any two questions.

Section-A

1.

a) What are various capabilities of VHDL?
b) Explain VHDL design flow with an example?
c) Explain various multiplying operators in VHDL with examples?
d) How does PLA different from ROM?
e) Define Generate, Guarded Block, and Assert statements in VHDL.
f) Differentiate between behavioral and dataflow style of circuit modeling.
g) What are various CAD tools for digital circuit design?
h) What are PULL UP and PULL DOWN networks?
i) What are transport and inertial delays in VHDL?
j) What are Generics?

Section-B

2. Design a Full adder using two half adders. Implement this Full adder using VHDL Code.
3. Write a VHDL Code to implement the function

$$f(x1,\ldots, x4) = \prod M\ (3, 11, 14) + D\ (0, 2, 10, 12).$$

4. Write a VHDL code for BCD to 7- Segment decoder using CASE statement.

5. Write a VHDL description of the following combinational network in Fig.1 concurrent statements. Each gate has a 5-ns delay, excluding the inverter, which 2-ns delay.

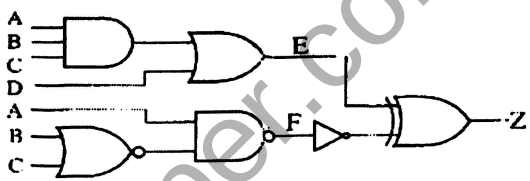

Fig.1

6. Write VHDL Code using behavioral modeling style that represents a T-flip- flo an asynchronous clear input.

Section-C

7. a) Implement the CPU of a basic computer using VHDL. This CPU is to perf least arithmetic and logical functions on an 8-bit data.

   b) What are programmable logic devices? Explain architecture of a general FPGA

8. Design a 3- bit UP/Down counter using T-Flip Flops. It should include a control called $\overline{UP}$/Down. If $\overline{UP}/Down$ =0. then the circuit should behave as an up-cour $\overline{UP}/Down$ =1, then the circuit should behave as a down counter. Implement thi UP/Down Counter using VHDL Code.

9. Draw the CMOS inverter and discuss its DC characteristics. Write the conditic different regions of operation.

End