Roll No. $\square$ Total No. of Pages: 02
Total No. of Questions : 09

# B.Tech.(CSE / IT) (Sem.-3) <br> DIGITAL CIRCUITS AND LOGIC DESIGN <br> Subject Code : CS-205 <br> Paper ID : [A0453] 

Time : 3 Hrs.
Max. Marks : 60

## INSTRUCTION TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students has to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students has to attempt any TWO questions.

## SECTION-A

1. Write briefly :
a) Define the term Decoder.
b) Convert SOP expression $\left(\mathrm{AB}+\mathrm{BC}^{\prime}+\mathrm{C}^{\prime} \mathrm{D}\right)$ in to its equivalent POS form.
c) Represent (-11) in 2's complement form using 5 bits.
d) What is difference between multiplexer and demultiplexer?
e) What do you understand by Shift Registers?
f) Name any two Analog to Digital Converters.
g) What is the reason behind using gray code in K-Map?
h) Subtract $(1101)_{2}$ from $(1001)_{2}$ using 2 's complement subtraction.
i) What is the state of JK flipflop when both the inputs are high (i.e. when $\mathrm{J}=1 . \mathrm{K}=1$ )?
j) Differentiate between synchronous and asynchronous counters.

## SECTION B

2. Reduce the following expression using K-map method and specify the Selective Prime Implicant (SPI), Redundant Prime Implicant (RPI), and Essential Prime Implicant (EPI).
$\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D})=\sum \mathrm{m}(1,5,6,7,11,12,13,15)$
3. What is excitation table? Design JK flip flop from SR flip flop by the use of excitation table.
4. Convert following number system
a) $(12.25)_{10}=(?)_{2}$
b) $(10101.1101)_{2}=(?)_{16}$
c) $(125)_{8}=(?)_{10}$
d) $(34)_{16}=(?)_{2}$
e) $(67.2)_{8}=(?)_{2}$
5. Design 3-bit synchronous counter using JK flip flop. Also draw the counting sequence for the same.
6. What is the application of digital to analog converter? Explain $\mathrm{R} / 2 \mathrm{R}$ ladder digital to Analog Converter with neat diagram.

## SECTION C

7. What is programmable logic array? Implement programmable logic array (PLA) for given functions:
$\mathrm{F} 1=\mathrm{AB}^{\prime}+\mathrm{AC}+\mathrm{A}^{\prime} \mathrm{BC}^{\prime}$
$\mathrm{F} 2=\mathrm{AC}+\mathrm{BC}$
8. a) Design a 3 bit Gray to Binary code converter.
b) Design a 3 bit even parity generator and show its truth table.
9. a) Distinguish between a half adder and a full adder with the help of truth table and logic diagram.
b) With the help of logic diagram and truth table, explain an octal to binary encoder.
