Roll No. ⬚⬚⬚⬚⬚⬚⬚⬚⬚⬚⬚   Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(CSE) / (IT)   (Sem.–3)
# COMPUTER ARCHITECTURE
Subject Code : CS-201
Paper ID : [A0451]

Time : 3 Hrs.   Max. Marks : 60

INSTRUCTION TO CANDIDATES :
1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students has to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students has to attempt any TWO questions.**

SECTION-A

1.   **Write briefly :**

a) What is an instruction set? How many different instructions MP 8085 has?

b) A computer uses RAM chips of 1024×8 capacity. How many chips are needed to provide a memory capacity of 64KB?

c) What are the steps taken when an interrupt occurs?

d) How Layered architecture of computer system affects the cost?

e) Perform the Logic AND, OR and XOR with the two binary numbers 10011100 and 10101010.

f) What is Von Neumann architecture?

g) Distinguish between Static RAM and Dynamic RAM.

h) List the four types of I/O commands received by input-output interface.

i) What are the cons and pros of using hardwired control unit over micro-programmed control unit?

j) Which data and instruction organization support parallelism? Explain with the help of example.

SECTION-B

2. Show the step by step multiplication process, using Booth's algorithm to multiply two numbers 17 * (-7).

3. Differentiate RISC and CISC microprocessors.

4. Draw and explain the circuit of Look Ahead carry Generator.

5. Discuss the performance evaluation LINPACK Whetstone and Dhrystone.

6. An instruction is stored at location 400 with its address field at location 401. The address field has the value 200. A processor register R1 contains the number 350. The content at location 200 is 105. Evaluate the effective address if the addressing mode of the instruction is :

   (a) Direct   (b) immediate

   (c) PC Relative   (d) Index with R1 as the index register

   (e) Indirect

SECTION - C

7. What is an Instruction cycle? Draw a complete flowchart of an instruction cycle showing its different phases. (10)

8. (a) An address space is specified by 20 bits and corresponding memory space by 16 bits.

   i)   How many words are there in the address space and in the memory space? (2)

   ii) If a page consists of 2K words, how many pages and blocks are there in the system? (3)

   (b) What are the different types of mapping procedures when considering the organization of cache memory? Explain one mapping procedure in detail with a diagram. (5)

9. How DMA controller communicates with CPU & I/O devices? Explain with a block diagram of DMA controller. How DMA Controller is different from Input-Output processor (IOP)? (10)