**Roll No.** | | | | | | | | | | | | **Total No. of Pages : 02**

**Total No. of Questions : 07**

**BCA (2011 & Onward) (Sem.–2)**

# COMPUTER SYSTEM ARCHITECTURE

**Subject Code : BSBC-204**

**Paper ID : [B1116]**

**Time : 3 Hrs.** **Max. Marks : 60**

**INSTRUCTION TO CANDIDATES :**

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains SIX questions carrying TEN marks each and a student has to attempt any FOUR questions.**

## SECTION-A

**1. Write briefly :**

a. What is difference between computer organisation and computer architecture?

b. What do you mean by the micro-operation?

c. Define the concept of BUS.

d. What do you mean by an interrupt?

e. Write note on control unit.

f. What do you mean by computer memory? Which is the fastest memory of computer?

g. Write full name for the following terms : RAM, DMA, LRU, FIFO.

h. Define the term associative memory.

i. What is the addressing mode? Write difference between direct and indirect addressing modes.

j. Define the mobile devices architecture in brief.

## SECTION-B

2. Explain the concept of stored program computer. Give Von Neumann architecture for it.

3. What are the basic operations that are carried out in registers? Given 8-bit registers AR, BR, CR and DR such that AR = 11110010, BR = 11111111, CR = 10111001

   DR = 11101010, determine the 8-bit values in each register after execution of following sequence of micro- operations :

   a. AR ←AR + BR

   b. BR ← BR + 1

   c. CR ←CR ^ DR

   d. AR ←AR + BR

4. Explain the instruction cycle and its different phases. Also draw the flow chart for instruction cycle.

5. Explain how I/O data transfer takes place with the help of DMA. In what ways is it better than other I/O data transfer techniques? Discuss with example.

6. What do you mean by cache memory? Discuss the role of cache memory. Explain various mapping procedures/ techniques used for cache memory organisation.

7. Differentiate the following :

   a. Hardwired and micro programmed control unit

   b. LRU and FIFO page replacement algorithms.