Roll No. | | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech.(CSE/IT) (2011 onwards)

B.Tech.(3D Animation & Graphics) (2012 onwards)

(Sem.–3)

COMPUTER ARCHITECTURE

Subject Code : BTCS-301

Paper ID : [A1123]

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1) Write briefly :

a) What are the basic functional units of a computer?

b) Draw the block diagram of a 2's complement Subtractor.

c) Explain the concept of virtual memory.

d) Discuss the different types of ROMs.

e) What is Inter-process communication?

f) Draw a schematic diagram of the memory hierarchy.

g) What is a priority Interrupt?

h) Briefly discuss the basic organization of a micro programmed control unit.

i) The address of a memory location to be accessed is in register R_1 and the memory data are to be loaded into register R_2. Specify the sequence of operations involved.

j) Differentiate serial and parallel communication.

SECTION-B

Q2) Explain in detail the CISC architecture.

Q3) Briefly outline the concept of auxiliary memory and associative memory.

Q4) Why page-table is required in a virtual memory system? Explain different ways of organizing a table.

Q5) Explain, in detail the various addressing modes of Central Processing Unit.

Q6) Briefly explain the concept of synchronization in context of inter-process communication.

SECTION-C

Q7) Explain instruction cycle. Give the RTL statement for each sub cycle. How the instruction cycle is to accommodate the interrupt from I/O devices?

Q8) Explain how cache memory is different from virtual memory. Also, discuss various page replacement policies for virtual memory with examples.

Q9) Write short notes on :

a) DMA

b) Stack organization