

SECTION-B

2. Design an 8 : 3 Priority Encoder. Implement the priority encoder using VHDL code.
3. Write VHDL code for a full subtractor using logic equations.
4. Write a VHDL Code to implement the function

$$F(x_1, \dots, x_4) = \sum m(1, 4, 7, 14, 15) + D(0, 5, 9).$$

5. Design a string detector circuit that takes as input a serial bit stream and outputs a '1' whenever the sequence "111" occurs. Overlap must also be considered, that is, if 0111110... occurs, then the output should remain active for three consecutive clock cycles. Also write VHDL code for the same.

Input string is : "011101100"

6. Design a shifter circuit which can shift a four bit input vector, $W = w_3w_2w_1w_0$, one bit position to the right when the control signal Right is equal to 1, one bit position to the left when the control signal Left is equal to 1. When Right = Left = 0, the output of the circuit should be the same as the input vector. Assume that the condition Right = Left = 1 will never occur. Write VHDL code for the shifter.

SECTION-C

7. Draw the CMOS inverter and discuss its DC characteristics. Write the conditions for different regions of operation.
8. a) Implement the CPU of a basic computer using VHDL. This CPU is to perform atleast arithmetic and logical functions on an 8-bit data,
 b) What are programmable logic devices? Explain architecture of a general FPGA.
9. a) Write short note on :
 i) Constant Field Scaling
 ii) Constant Voltage Scaling
 b) Design a 3 bit twisted ring Counter. Write its VHDL Code