Roll No. | | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech.(CSE / IT) (Sem.–3)

DIGITAL CIRCUITS AND LOGIC DESIGN

Subject Code : CS-205

Paper ID : [A0453]

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1) Write briefly :

a) Convert $(574)_8$ to $()_{16}$.

b) Write $(-33)_{10}$ in 2's complement format.

c) Convert $(10110)_2$ to gray code.

d) What are the advantages of TTL family over RTL family?

e) Compare synchronous counters with asynchronous counters.

f) How sequential circuits are different from the combinational circuits?

g) What are universal gates?

h) What is resolution in D/A converter?

i) Design AND gate with 4:1 MUX.

j) What is a flip-flop?

SECTION-B

2) Simplify the following using K-map :

$$Y = \sum m(0,1,2,8,10) + d(3,5)$$

3) Design 4:1 MUX with the help of logic gates.

4) Design mod-8 synchronous counter using J-K flip-flops.

5) Draw and explain the operation of TTL inverter.

6) Write a short note on VLSI design.

SECTION-C

7) Design full adder with the help of logic gates.

8) Discuss the different types of semiconductor memories.

9) What is race-around condition? How it is eliminated in Master-Slave J-K flip-flop?