Roll No. | | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech.(CSE) / (IT) (Sem.–3)

COMPUTER ARCHITECTURE

Subject Code : CS-201

Paper ID : [A0451]

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Write briefly :

(a) Show with a block diagram how different components of a computer system are connected together.

(b) A computer uses memory unit of 512 words of 16 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code to specify one of 8registers and an address part. How many bits are there in each part?

(c) Perform the operation (–29) + (18) with binary numbers represented in signed 2's compliment form.

(d) Draw the bus architecture of 8085 MP.

(e) What are main characteristics of RISC processor architecture?

(f) How I/O devices communicate with each other?

(g) Define hit ratio.

(h) What do you mean by Transaction processing benchmark?

(i) List the operational modes of 8255 interface.

(j) Compare SIMD and MIMD machines.

SECTION-B

2. Explain all addressing modes used in a general computer system with example.

3. What are interrupts? What are the major types of interrupts?

4. Design hardware implementation for the signed 2's complement multiplication (Booth algorithm). Also draw flowchart for multiplication of two numbers represented by 2's compliment.

5. Write zero, one, two, three address instructions for the evaluation of following expression:

   $X = (A - B) + (C * D)$

6. In certain scientific computations it is necessary to perform the arithmetic operation $(A_i + B_i)*(C_i + D_i)$ with the stream of numbers. Specify the pipeline configuration to carry out this task. List the contents of all registers in the pipeline from i = l through 6.

SECTION-C

7. Represent the hardwired control unit of a basic computer consisting 3 × 8 and 4 ×16 decoder. Elucidate how it will work and generate control signals. (10)

8. (a) How DMA transfer takes place? Explain. (7)

   (b) Draw a block diagram of a Computer with Input-output processor. (3)

9. (a) The logical address space consists of 256 segments. Each segment can have up to 32 pages of 4K words each. Physical memory consists of 8K blocks of 4K words. Find the logical and physical address bits. Also formulate the logical and physical address format. (4)

   (b) Write a short note on memory hierarchy in a computer System. Compare cache and main memory. (6)