Roll No. | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech.(CSE)/(IT) (2011 Onwards) (Sem.–3)

DIGITAL CIRCUITS & LOGIC DESIGN

Subject Code : BTCS-303

Paper ID : [A1125]

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Write briefly :

a) Explain the K-map reduction technique.

b) Write a short note on ASCII code.

c) Explain the ECL circuit.

d) Calculate the number of select lines in 16 to 1 multiplexer?

e) Explain the NOR Gate. Specify its symbol.

f) Built a full adder from half adder circuits.

g) List any four characteristics of logic gates.

h) Convert decimal 177.25 to octal number.

i) Compare between TTL and CMOS logic.

j) Write the applications of EX–OR gate.

SECTION-B

2. What is the necessity of Interfacing in digital ICs and what are the points to be kept in view, while interfacing between TTL gate and CMOS gate?

3. Minimize the following expression using K–map.

   $Y = \Sigma m\ (0, 1, 2, 5, 13, 15)$

4. Draw a typical connection diagram for DAC 0808 and explain it.

5. Write a short note on the following :

   a) FPGA

   b) EPROM.

6. What is full subtractor? Draw a full subtractor circuit.

SECTION-C

7. a) Draw the logic diagram of 4–bit Twisted Ring counter and explain its operation with the help of timing diagram.

   b) Design a MoD–3 synchronous counter using J–K Flip–Flops.

8. a) Explain how Parallel in Serial Out (PISO) shift register works.

   b) Design a mod-6 up counter.

9. a) Explain how EPROM memory cell works.

   b) Explain the working of dual slope A/D converter.